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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/602,901	06/23/2000	James R. Peterson	500689.01	9313

27076 7590 12/13/2002

DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101

EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 12/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/602,901	Applicant(s) PETERSON ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-18, 31-39 are rejected under 35 U.S.C. 102(a) as being anticipated by Cox (U.S. Patent No. 5,357,621).

Referring to claims 1 and 4, Cox teaches an expandable memory system for use in a computing system which comprises a plurality of plug-in memory modules coupled to a memory system controller in a serial network. The memory system network consists of a central memory system controller and at least one individually addressable memory module controller coupled serially to the memory system controller. Various command signals generated by the memory system controller and information or data signals generated either by the memory system controller or individual memory module controllers in response to commands transmitted from the system controller, are transmitted and received serially between the system controller and the memory module controllers (col. 2, lines 36-50). The expandable memory system of the present invention utilizes a plurality of plug-in, add-on memory modules or memory cards wherein each individual memory module comprises a module controller, a module memory address control logic block and at least one memory block having a number of individually addressable memory cells (col. 2, lines 53-59). The system also includes the capability to bypass or disable bad

memory modules and reassign memory addresses without leaving useable memory unallocated (col. 3, lines 37-39).

In regard to claims 2, 3 and 5, as shown in Fig. 2, Cox teaches each individual memory module 20 comprises a module MCL controller 22, memory address control logic 21 (programmable array logic blocks) and one or more blocks of memory 23, 25, 27 and 29, each memory block comprising, for example, a 256 k-byte dynamic random access memory (DRAM) array (col. 4, lines 21-26). The real time logical combination between the physical address on bus 37b and the base address on bus 35 coupled with the DRAM column address strobe on bus 37a via the memory address control logic 21 provides the selection of the appropriate memory blocks 23, 25, 27 and 29 (col. 6, lines 20-26). Thus, the memory address control logic 21 stores and controls the functional memory blocks 23, 25, 27 and 29 through the column address strobes (CAS1-CAS-n) (Fig. 2).

Referring to claim 6, Cox teaches upon power up, the memory system controller automatically configures the memory system assigning an address to each of the memory module controllers in the network and a base address for the memory on each of the memory modules in the system (col. 2, lines 65-68, and col. 3, lines 1-2).

In regard to claim 7, Cox teaches the starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module. The process is repeated for each memory module 20 in turn until the entire memory space is defined. The starting addresses that are assigned to each of the individual memory modules 20 are referred to as base addresses. A specific memory

module 20 will respond to addresses defined from [BASE] to [BASE+SIZE] (col. 5, lines 33-43).

Referring to claims 8-11, 14-17, as cited above, Cox teaches a memory system comprising plurality of memory modules, each of which includes a plurality of memory blocks (sub-arrays) memory blk 1-memory blk n as shown in Fig. 2; a memory address control logic 21 coupled to each individual memory blocks 1-n through column address strobes (CAS1-CASn, respectively); and a memory controller 22 coupled to the memory address control logic 21 to access the respective memory block for memory access request. Memory blocks are DRAM arrays embedded in the memory modules.

In regard to claims 12-13, as cited above, Cox teaches the system controller assigns the base address memory to each module controller and start value of the next module is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module.

As for claim 18, Cox teaches the Memory Address Mask command (Opcode 40-4F) is utilized to assign the base address for the first memory module on the control link. The mask value corresponds to the upper 4 bits of actual addresses in a 16 megabyte memory system where a 1-megabyte block of memory equals 1 mask value. The mask command values range from 40 to 4F. The 0 to F hexadecimal values define the absolute starting block address in increments of 1 megabyte per block. If more than 1 megabyte of memory exists on a given memory module, the MCL controller 22 will sequentially build additional addressing for each additional block of 1 megabyte of memory (col. 10, lines 1-13). Thus, Opcode 40-4F is used to keep track of the number of functional sub-arrays in the memory module.

Referring to claims 31, as cited above, Cox teaches a memory system comprising plurality of memory modules, each of which includes a memory array segmented into plurality of memory blocks (sub-arrays). Upon power up, the memory system controller automatically configures the memory system assigning an address to each of the memory module controllers in the network and a base address for the memory on each of the memory modules in the system (col. 2, lines 65-68, and col. 3, lines 1-2). Also, Cox teaches while the system controller 11 attempts to provide contiguous memory, it is not required that the memory space may be defined with all address blocks assigned. Additional blocks of memory may be defined anywhere within the memory space if desired or necessary. Similarly, undefined blocks or space may be left in the memory space if necessary, for example, to bypass a failed memory block (col. 5, lines 26-33). Cox further teaches the system DRAM controller 33 provides the appropriate signals for controlling the individual memory blocks 23, 25, 27, 29 during real time memory accesses by the host system (col. 4, lines 65-68).

In regard to claim 32, as mentioned above, Cox teaches the memory address control logic 21 coupled to each individual memory blocks 1-n through column address strobes (CAS1-CASn, respectively).

As for claim 33, as cited above, Cox teaches Opcode 40-4F is used to keep track of the number of functional sub-arrays in the memory module.

In regard to claim 34, as cited above, Cox teaches the memory blocks 23-29 are DRAM embedded memory arrays.

Referring to claims 35 and 36, as cited above, Cox teaches the memory module is first assigned start address and size, and the memory system can either bypass or disable bad memory

modules. Also cited above, Cox teaches the starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module.

Referring to claims 37-39, as cited above, Cox teaches a memory system with multiple memory controllers comprising plurality of memory blocks of DRAM arrays wherein upon power up, the system controller assigns the start address and size to each individual memory controllers, and the DRAM controllers 33 provides the appropriate signals for controlling the individual memory blocks 23, 25, 27, 29 during real time memory accesses by the host system. If any bad memory module is recognized, the system can either bypass or disable that module. Also cited above, Cox teaches the starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module; and the command Opcode (40-4F) keeps track of the number of the functional memory sub-array.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox (U.S. Patent No. 5,357,621) in view of Jeddeloh (U.S. Patent No. 6,252,612).

Referring to claims 19-22, 26-29, as cited above, Cox teaches a memory system comprising plurality of memory modules, each of which includes a plurality of memory blocks (sub-arrays) memory blk 1-memory blk n as shown in Fig. 2; a memory address control logic 21 coupled to each individual memory blocks 1-n through column address strobes (CAS1-CASn, respectively); and a memory controller 22 coupled to the memory address control logic 21 to access the respective memory block for memory access request. Memory blocks are DRAM arrays embedded in the memory modules.

Thus, Cox teaches all the limitations of claims 19-22, 26-29, except for the memory system is configured in a graphic processing system wherein, a graphic processor is coupled to the system bus, and address and data busses coupled to the graphic processor to transfer addresses and data to and from the graphic processor; and a display driver coupled to data bus.

However, Jeddeloh teaches a computer, comprising at least one processor; and at least two memory controllers, wherein one of the at least two memory controllers includes an accelerated graphics port and at least one configuration register defining a range of addresses that are available for accelerated graphics port transactions (col. 3, lines 36-42). As shown in Fig. 2, Jeddeloh teaches the computer 150 includes at least one processor 152 connected to a first memory controller 154 and a second memory controller 155 by a processor or host bus. The computer 150 also has a first main memory 156 and a second main memory 157 connected to the first memory controller 154 and the second memory controller 155, respectively. A graphics accelerator 160 communicates with a local frame buffer 162 and the first memory controller 154

through an accelerated graphics port (AGP) 166. The AGP 166 is a point-to-point connection between the first memory controller 154 and the graphics accelerator 160. The first memory controller 154 and the second memory controller 155 also accept memory requests from a PCI bus 158 (col. 4, lines 5-26).

Therefore, it would have been obvious to one skilled in the art to utilize graphic system as taught by Jeddeloh in combination with the memory system as taught by Cox in order to improve methods for storing, addressing and retrieving graphics data from main memory and reduce the system cost of high bandwidth graphics applications (col. 3, lines 20-26).

In regard to claims 23 and 30, as cited above in claim 18, Cox teaches the Memory Address Mask command (Opcode 40-4F) of the command Opcodes is utilized to keep track of the number of functional memory blocks in the memory module.

As for claims 24-25, as cited above, Cox teaches the system controller assigns the base address memory to each module controller and start value of the next module is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

6. Johnson et al. (U.S. Patent No. 4,507,730) disclose a memory system with multiple memory controllers wherein when a memory fault is detected by the data processing unit, the

memory controllers are reconfigured by predetermined types of commands specifying reconfiguration.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

12/10/2002

Matthew C. Bella
Primary Examiner